CLAIMS

1. An input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal; and

a voltage generator having an output terminal coupled to the reference terminal and further having a control terminal coupled to the output of the input buffer, the voltage generator generating as the reference voltage signal an output signal having a voltage dependence on the logic value of the output signal of the input buffer.

2. The input stage of claim 1 wherein the voltage generator comprises an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal a high reference voltage signal at the first output terminal and a low reference voltage signal at the second output terminal.

3. The input stage of claim 2 wherein the amplifier comprises:

an operational amplifier having a first input at which the initial reference voltage is applied, a second input, and an output at which an output signal is provided; and

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which the high reference voltage is provided, a second node coupled to the second input of the operational amplifier, and a third node at which the low reference voltage is provided.

4. The input stage of claim 2, further comprising a multiplexer having a selection terminal coupled to the output of the input buffer, an output coupled to the reference terminal, and first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, the multiplexer providing the high reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a low logic value and the low reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a high logic value.

5. The input stage of claim 2, further comprising first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

6. The input stage of claim 2, further comprising a first capacitor having a first terminal coupled to the first output terminal of the amplifier and a second capacitor having a first terminal coupled to the second output terminal of the amplifier, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

7. An input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal;

an operational amplifier having a first input at which an initial reference voltage is applied, a second input, and an output;

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which a high reference voltage is provided, a second node coupled to the second input of the operational amplifier, and a third node at which a low reference voltage is provided; and

first and second transfer gates coupled to the first and second nodes of the voltage divider, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

8. The input stage of claim 7, further comprising a first capacitor having a first terminal coupled to the first node and a second capacitor having a first terminal coupled to the third node, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

9. The input stage of claim 7 wherein the voltage divider comprises:

a first resistor electrically coupled between the output of the operational amplifier and the first node;

a second resistor electrically coupled between the first node and the second node;

a third resistor electrically coupled between the second node and the third node; and

a fourth resistor electrically coupled between the third node and the reference voltage supply.

10. The input stage of claim 7, further comprising first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

11. An input stage including an SSTL input buffer having input signal terminal, an output terminal and a reference voltage terminal, the input stage comprising:

an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal a high reference voltage signal at the first output terminal and a low reference voltage signal at the second output terminal; and

a selection circuit having first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, an output terminal coupled to the reference voltage terminal, and a control terminal coupled to the output terminal of the input buffer, the selection circuit selectively coupling the first and second input terminals to the output terminal based on a logic value of an output signal of the input buffer to provide either the high or low reference voltage signals to the input buffer as the reference voltage signal.

12. The input stage of claim 11 wherein the amplifier comprises:

an operational amplifier having a first input at which the initial reference voltage is applied, a second input, and an output at which an output signal is provided; and

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which the high reference voltage signal is provided, a second node coupled to the second input of the operational amplifier, and a third node at which the low reference voltage signal is provided.

13. The input stage of claim 12 wherein the voltage divider comprises:

a first resistor electrically coupled between the output of the operational amplifier and the first node;

a second resistor electrically coupled between the first node and the second node;

a third resistor electrically coupled between the second node and the third node; and

a fourth resistor electrically coupled between the third node and the reference voltage supply.

14. The input stage of claim 11 wherein the selection circuit comprises a multiplexer having a selection terminal coupled to the output terminal of the input buffer, an output coupled to the reference terminal, and first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, the multiplexer providing the high reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a low logic value and the low reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a high logic value.

15. The input stage of claim 11 wherein the selection circuit comprises first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

16. The input stage of claim 11, further comprising a first capacitor having a first terminal coupled to the first node and a second capacitor having a first terminal coupled to

the third node, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

17. An input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal; and

first and second voltage supplies providing first and second voltage levels, respectively; and

a selection circuit having first and second input terminals coupled to the first and second voltage supplies, respectively, an output terminal coupled to the reference terminal, and a control terminal coupled to the output terminal of the input buffer, the selection circuit selectively coupling the first and second input terminals to the output terminal based on the logic value of the output signal of the input buffer to provide either the first or second voltage levels as the reference voltage signal.

18. The input stage of claim 17 wherein the first and second voltage supplies comprise an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal the first voltage level at the first output terminal and the second voltage level at the second output terminal.

19. The input stage of claim 18 wherein the amplifier comprises:

an operational amplifier having a first input at which the initial reference voltage is applied, a second input, and an output at which an output signal is provided; and

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which the first voltage level is provided, a second node coupled to the second input of the operational amplifier, and a third node at which the second voltage level is provided.

20. The input stage of claim 17 wherein the selection circuit comprises a two-input multiplexer.

21. The input stage of claim 17 wherein the selection circuit comprises first and second transfer, each gate having an input terminal coupled to a respective voltage supply and further having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the first voltage level to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the second voltage level to the reference terminal in response to the output signal of the input buffer having a high logic value.

22. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to

which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal; and

a voltage generator having an output terminal coupled to the reference terminal and further having a control terminal coupled to the output of the input buffer, the voltage generator generating as the reference voltage signal an output signal having a voltage dependence on the logic value of the output signal of the input buffer.

23. The memory device of claim 22 wherein the voltage generator of the input stage comprises an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal a high reference voltage signal at the first output terminal and a low reference voltage signal at the second output terminal.

24. The memory device of claim 23 wherein the amplifier of the input stage comprises:

an operational amplifier having a first input at which the initial reference voltage is applied, a second input, and an output at which an output signal is provided; and

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which the high reference voltage is provided, a second node coupled to the second input of the operational amplifier, and a third node at which the low reference voltage is provided.

25. The memory device of claim 23 wherein the input stage further comprises a multiplexer having a selection terminal coupled to the output of the input buffer, an output coupled to the reference terminal, and first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, the multiplexer providing the high reference voltage signal as the reference voltage signal in response to the output signal of the

input buffer having a low logic value and the low reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a high logic value.

26. The memory device of claim 23 wherein the input stage further comprises first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

27. The memory device of claim 23 wherein input stage further comprises a first capacitor having a first terminal coupled to the first output terminal of the amplifier and a second capacitor having a first terminal coupled to the second output terminal of the amplifier, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

28. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal; and

a voltage generator having an output terminal coupled to the reference terminal and further having a control terminal coupled to the output of the input buffer, the voltage generator generating as the reference voltage signal an output signal having a voltage dependence on the logic value of the output signal of the input buffer.

29. The computer system of claim 28 wherein the voltage generator of the input stage comprises an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal a high reference voltage signal at the first output terminal and a low reference voltage signal at the second output terminal.

30. The computer system of claim 29 wherein the amplifier of the input stage comprises:

an operational amplifier having a first input at which the initial reference voltage is applied, a second input, and an output at which an output signal is provided; and

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which the high reference voltage is provided, a second node coupled to the second input of the operational amplifier, and a third node at which the low reference voltage is provided.

31. The computer system of claim 29 wherein the input stage further comprises a multiplexer having a selection terminal coupled to the output of the input buffer, an output coupled to the reference terminal, and first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, the multiplexer providing the high reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a low logic value and the low reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a high logic value.

32. The computer system of claim 29 wherein the input stage further comprises first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

33. The computer system of claim 29 wherein input stage further comprises a first capacitor having a first terminal coupled to the first output terminal of the amplifier and a second capacitor having a first terminal coupled to the second output terminal of the amplifier, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

34. A method for generating an output signal having a logic level in response to receiving an input signal having a voltage level, the method comprising:

comparing the voltage level of the input signal to a first reference voltage when the current output signal has a first logic level;

comparing the voltage level of the input signal to a second reference voltage when the current output signal has a second logic level; and

switching between the first and second reference voltages in response to the logic level of the output signal changing.

35. The method of claim 34, further comprising:

generating from an initial reference voltage the first reference voltage having a voltage relatively greater than the voltage of the initial reference voltage; and

generating from the initial reference voltage the second reference voltage having a voltage relatively lower than the voltage of the initial reference voltage.

36. The method of claim 35 wherein the first logic level comprises a LOW logic level and the second logic level comprises a HIGH logic level.

37. The method of claim 35 wherein switching between the first and second reference voltages comprises:

selecting the relatively lower reference voltage for comparison in response to the output signal having the HIGH logic level; and

selecting the relatively greater reference voltage in response to the output signal having the first LOW logic level.

38. A method for generating an output signal having a logic level in response to receiving an input signal having a voltage level, the method comprising:

generating a variable reference voltage to which the voltage level of the input signal is compared;

comparing the voltage level of the input signal to the voltage level of the variable reference voltage to determine the logic level of the output signal; and

adjusting the voltage level of the variable reference voltage in response to the logic level of the output signal changing.

39. The method of claim 38 wherein adjusting the voltage level of the variable reference voltage comprises:

selecting a first reference voltage for comparison in response to the output signal having the second logic level; and

selecting a second reference voltage for comparison in response to the output signal having the first logic level.

40. The method of claim 39 wherein the first voltage level is a relatively higher voltage than an initial reference voltage and the second voltage level is a relatively lower voltage than the initial reference voltage, the first voltage level is a HIGH logic level, and the second voltage level is a LOW logic level.

41. The method of claim 38 wherein generating a variable reference voltage comprises:

generating from an initial reference voltage a first voltage against which the voltage level of the input signal is compared, the voltage of the first voltage relatively greater than the voltage of the initial reference voltage; and

generating from the initial reference voltage a second voltage against which the voltage level of the input signal is compared, the voltage of the second voltage relatively lower than the voltage of the initial reference voltage.

42. The method of claim 38 wherein comparing the voltage level of the input signal comprises:

when the voltage level of the input signal is greater than a first voltage level, generating an output signal having a first logic level; and

when the voltage level of the input signal is less than a second voltage level, generating an output signal having a second logic level, the second voltage level unequal to the first voltage level.

43. A method for generating an output signal having a logic level in response to receiving an input signal having a voltage level, the method comprising:

when the voltage level of the input signal is greater than a first voltage level, generating an output signal having a first logic level;

when the voltage level of the input signal is less than a second voltage level, generating an output signal having a second logic level, the second voltage level unequal to the first voltage level; and

switching between the first and second voltage levels when the logic level of the output signal changes.

44. The method of claim 43 wherein switching between the first and second reference voltages comprises:

selecting the first reference voltage in response to the output signal having the second logic level; and

selecting the second reference voltage in response to the output signal having the first logic level.

45. The method of claim 43 wherein the first voltage level is a relatively higher voltage than an initial reference voltage and the second voltage level is a relatively lower voltage than the initial reference voltage, the first voltage level is a HIGH logic level, and the second voltage level is a LOW logic level.

46. The method of claim 43, further comprising:

generating from an initial reference voltage the first voltage level having a voltage relatively greater than the voltage of the initial reference voltage; and

generating the second voltage level having a voltage relatively lower than the voltage of the initial reference voltage.